REMARKS

Favorable reconsideration of this application is respectfully requested.

The specification is amended by the present response to correct minor informalities therein. No new matter is believed to be added.

Claims 1-20 are pending in this application. Claims 1-3, 6-7, 12-13, and 16-20 were rejected under 35 U.S.C. § 102(e) as anticipated by U.S. patent 7,098,685 to Agrawal et al. (herein "Agrawal"). Claims 4-5, 8-11, and 13-14 were rejected under 35 U.S.C. § 103(a) as unpatentable over Agrawal as applied to claim 1, in view of U.S. Patent Application Publication 2003/0196139 A1 to Evans. Claims 13, 15, and 20 were rejected under 35 U.S.C. § 103(a) as unpatentable over Agrawal as applied to claims 1 and 2, in view of U.S. patent 5,742,798 to Goldrian. Those rejections are traversed by the present response as discussed next.

Initially, applicants note each of independent claims 1 and 12 is amended by the present response to clarify features recited therein. Independent claim 1 now further recites a "first serializer which converts parallel data into serial data synchronized with a transmit clock in a normal operation and a first test operation, and which converts the parallel data into the serial data synchronized with the clock generated by the first clock data recovery circuit in a second test operation". Independent claim 1 now also further recites "a second serializer which converts parallel data into serial data synchronized with a transmit clock in the normal operation and the second test operation, and which converts the parallel data into the serial data synchronized with the clock generated by the second clock data recovery circuit in the first test operation". Independent claim 12 is amended by the present response to recite similar features. The above-noted claim features are believed to be fully supported by the original specification. As a non-limiting example a normal operation is noted in the present specification at page 11, lines 11-17 and Figure 2. Further, the first and second test

operations are supported by the original specification for example at page 13, line 24 to page 14, line 1, page 14, line 18 to page 15, line 1, and Figure 3.

Attached to the present response Applicants provide an Attachment summarizing different operations in the claims and the applied art.

First, in independent claims 1 and 12, during a second test operation a first serializer converts parallel data into serial data synchronized with a clock generated by a first clock data recovery circuit. Further, during a first test operation a second serializer converts parallel data into serial data synchronized with a clock generated by a second clock data recovery circuit. As shown in the Attachment, the primary reference to Agrawal does not disclose or suggest the above-described structure.

The outstanding rejection cites Agrawal at column 4, lines 31-36 to disclose a "first transmitter including a first serializer". At that portion Agrawal states a "transmitter and serializer serialize a parallel data into serial data stream operating at the high speed clock rate (supplied by PLL)". That is, in Agrawal the parallel data signal input to the transmitter and serializer merely operates in synchronism with a high speed clock supplied from the PLL, and that parallel data is not synchronized by a clock (E-RCK) generated by the receiver RCVR. In such ways independent claims 1 and 12 and believed to clearly distinguish over Agrawal.

Moreover, Evans does not disclose any features that cure the above-noted deficiencies in Agrawal. In that respect applicants also note in Figures 18A and 19A of Evans noted in the Office Action the arrows between 200 indicate a flow of serial data, and do not indicate a clock, as evident from Figure 18A of Evans, which is reprinted on the attachment. Further, Evans does not disclose or suggest synchronization of a data signal with a clock generated by an RX.

In view of these foregoing comments applicants respectfully submit each of amended independent claims 1 and 12, and the claims dependent therefrom, clearly distinguish over Agrawal, and further in view of Evans. Further, no teachings in Goldrian cure the above-noted deficiencies of Agrawal in view of Evans, and thus claims 13 and 15 dependent on claim 12 are also believed to distinguish over Agrawal in view of Goldrian.

Further, with respect to independent claim 20, independent claim 20 indicates when a first receiver is tested, a second transmitter transmits serial data synchronized with a phase-change clock output from a second recovery circuit, and when the second receiver is tested, the first transmitter transmits serial data synchronized with the phase-change clock output from the first recovery circuit. Those features are similar to above-discussed features in independent claims 1 and 12 that are believed to clearly distinguish over the applied art.

Moreover, in the method of claim 20, when the first receiver is tested, the second clock data recovery circuit changes a phase of the clock regardless of serial data, and when the second receiver is tested, the first clock data recovery circuit changes a phase of a clock regardless of serial data. That is, the first and second clock data recovery circuits generate clocks independently of the data transmitted from the second and first transmitters, respectively.

In contrast claim 20, in Goldrian the signal CLOCK_A in Figure 2, as an example, is generated based on the DATA_B transmitted from a driver module 211, and the signal CLOCK_B is generated based on the DATA_A transmitted from a driver module 210 (see Goldrian at column 5, lines 30-45).

In such ways Goldrian does not provide any disclosures that cure the deficiencies in Agrawal with respect to independent claim 20.

In view of the present response applicants respectfully submit the claims as currently written distinguish over the applied art.

As no other issues are pending this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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